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10/522,083	01/21/2005	Bernardo De Oliveira Kastrup Pereira	260683	7578

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EXAMINER	
DENG, ANNA CHEN	
ART UNIT	**PAPER NUMBER**
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,083	DE OLIVEIRA KASTRUP PEREIRA ET AL.	
	Examiner	Art Unit	
	Anna Deng	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on 1/21/2005.

2. Claims 1-19 are pending.

Specification

3. The abstract of the disclosure is objected to because exceeding 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 1 is objected to because of misusing semicolon in the preamble (line 1), it should be a comma. Appropriate correction is required.

5. Claim 10 is objected to because of missing a period at the end of the claim.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claim 19 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 19 set forth a partitioning compiler program product that is computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F. 3d at 1583-84, 32 USPQ2d at 1035. (see MPEP 2106.01 "Computer-Related Nonstatutory Subject Matter") .

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-19 are rejected under 35 U.S.C. 102 (e) as being anticipated by Aubury US 2003/0140337 A1 (hereinafter Aubury).

Per Claim 1:

Aubury discloses:

- **A method for partitioning a specification in a source code** ([0043], "provides a hardware/software codesign system which receives a specification of a target system in the form of behavioral description, i.e. a description in a programming language such as can be written by a computer programmer, and partitions it and compiles it to produce hardware and software"; [0044], "The partitioning means can include a parser for parsing the input behavioral description The description can be in a familiar computer language such as C, ... an obligatory partition to software or an obligatory partition to hardware"; emphasis added); **characterized in that the method comprises the following steps:**

- **converting the specification into a plurality of abstract syntax trees** (FIG. 4, [0122], "to turn the system description in the input language into an internal data structure, the abstract syntax tree which can be supplied to the partitioner 408");

- **partitioning the plurality of abstract syntax trees into at least a first set and a second set** ([0125],"The partitioner generates a control/data-flow graph from the abstract syntax tree,...It groups parts of the description together into blocks, "partitioning blocks"), **the first set of abstract syntax trees to be implemented by a first processor and the second set of abstract syntax trees to be implemented by a second processor** ([-126], The algorithms all assign each partitioning block to one of the hardware resources which has been declared"; [0082], "The resources may be a customizable processor, a fixed processor, or custom hardware").

Per Claim 2:

Aubury discloses:

- **wherein the second processor is a co-processor** (FIG. 22, [0034], "are determined for first and second processors for processing an application in operation 2202. Reconfigurable hardware is then configured in operation 2204 to provide at least one of the first and second processors such as programming a processor into a portion of an Field Programmable Gate Array (FPGA)", also, [0050], "a set of customizable (e.g. FPGA-based) processors").

Per Claim 3:

Aubury discloses:

- **wherein the first processor is a general-purpose processor** ([0049], "a fixed processor or processor core"; [0341], "at least one of the processors implemented in the reconfigurable hardware may designed by defining an instruction width, a width of internal memory and a stack address width; assigning processor opcodes; defining registers; ... and defining the processor based on the processor description").

Per Claim 4:

Aubury discloses:

- **converting the first set of abstract syntax trees to a first partial specification in the source code and converting the second set of abstract syntax trees to a second partial specification in the source code** ([0143], "the compile method on the hardware compiler class compiles the description to hardware by converting the input description on an RTL description, the compile method on the Processor A compiler compiles a description to machine code"; [0153], "The result of the hardware compilation ...is an RTL description which can be output to a RTL ... using a hardware description language(e.g., Handel-C or VHKL)"; [0163], "The output of the software compilation/processor parameterization process is machine code to run on the processor together with a description of the processor to be used").

Per Claim 5:

Aubury discloses:

- **wherein the step of partitioning the plurality of abstract syntax trees into a first set of abstract syntax trees and a second set of abstract syntax trees comprises a step of out-lining at least one abstract syntax tree based on profile data** (FIGS. 16-17, [0296], "for execution on a target system is profiled in operation 1702 utilizing a profiling tool for generating a profile of the model. Functions of the C executable model are analyzed in operation 1704 utilizing an analysis tool for estimating operations performed").

Per Claim 6:

Aubury discloses:

- **wherein the step of partitioning the plurality of abstract syntax trees into a first set of abstract syntax trees and a second set of abstract syntax trees comprises a step of out-lining at least one abstract syntax tree based on programmer provided information** (FIG. 18, [0303], "In operation, a plurality of profiling functions of a profiling process are selected. An application having application functions targeted for implementation in

reconfigurable logic is preprocessed in operation 1804 fro inserting calls to the selected profiling functions"; [0395], "Flow of control. ... The programmer has to decide which functions to call at what times for which kinds of objects").

Per Claim 7:

Aubury discloses:

- **A co-design method for producing a target system** ([0032], "provides a hardware/software codesign system which can target a system"), **wherein the target system comprises a first processor and at least a second processor** ([0048]-[0051], "The sort of target systems which can be produced include: a fixed processor or processor core, ... a set of customizable (e.g. FPGA-based) processors ... a system on a chip containing fixed processors and an FPGA");

- **the co-design method comprising the method for partitioning a specification in a source code according to claim 1** ([0032], "provides a hardware/software codesign system which can target a system in which the hardware or the processors to run the software can be customized according to the functions partitioned to it", emphasis added); also see discussion in claim 1, wherein all claimed limitations also have been addressed and or covered in cited areas as set forth above.

Per Claim 8:

Aubury discloses

- **converting the first set of abstract syntax trees to a first partial specification in the source code and converting the second set of abstract syntax trees to a second partial specification in the source code** ([0143], "the compile method on the hardware compiler class compiles the description to hardware by converting the input description on an RTL description, the compile method on the Processor A compiler compiles a description to

machine code"; [0153], "The result of the hardware compilation ...is an RTL description which can be output to a RTL ... using a hardware description language(e.g., Handel-C or VHKL)"; [0163], "The output of the software compilation/processor parameterization process is machine code to run on the processor together with a description of the processor to be used").

Per Claim 9:

Aubury discloses:

- **wherein the second processor is a co-processor** ([0050], "a set of customizable (e.g. FPGA-based) processors") **and wherein the second partial specification is converted to a specification of the co-processor** (FIG. 22, [0034], "are determined for first and second processors for processing an application in operation 2202. Reconfigurable hardware is then configured in operation 2204 to provide at least one of the first and second processors such as programming a processor into a portion of an Field Programmable Gate Array (FPGA)"; [0153], "an RTL description which can be output to a RTL synthesis system 414 using a hardware description language").

Per Claim 10:

Aubury discloses:

- **wherein the first processor is a general-purpose processor** ([0049], "a fixed processor or processor core") **and wherein the first partial specification is converted to object code by means of a compiler** ([0143], "the compile method on the hardware compiler class compiles the description to hardware by converting the input description on an RTL description, the compile method on the Processor A compiler compiles a description to machine code"; [0153], "The result of the hardware compilation ...is an RTL description which can be output to a RTL ... using a hardware description language(e.g., Handel-C or VHKL)"; [0163], "The output of the software compilation/processor parameterization process is

machine code to run on the processor together with a description of the processor to be used").

Per Claim 11:

Aubury discloses:

- **a step for defining an interface between the general-purpose processor and the co-processor** ([0039], "an interface generator for generating interfaces between the hardware and software").

Per Claim 12:

Aubury discloses:

- **wherein the specification of the co-processor comprises a specification of an ASIC** ([0039], "fixed hardware and a customizable processor. Thus, the customizable part could be formed on an FPGA, or for instance, an ASIC").

Per Claim 13:

Aubury discloses:

- **wherein the specification of the co-processor comprises a specification of a programmable processor** ([0043], "a description in a programming language such as can be written by a computer programmer, and partitions it and compiles it to produce hardware and software").

Per Claim 14:

Aubury discloses:

- **wherein the specification of the co-processor comprises a specification of a reconfigurable processor** ([0193], "the processor may be created in reconfigurable logic").

Per Claim 15:

Aubury discloses:

- **wherein the interface between the general-purpose processor and the co-processor comprises a remote function call** ([0198], "The system must dial up an Internet service provider, and establish a connection with the remote game, which will running on a workstation");

- **the remote function call having a set of parameters** ([0140], "Interfaces which are to be implemented using a resource which can be parameterized (such as a channel on an FPGA), are synthesized using the parameterizations decided by the partitioner");

- **the set of parameters comprising an identifier for the function to be called, at least one reference pointing to the input data of the function to be called and at least one reference pointing to the result data of the function to be called** ([0063], "an attribute may be added to input code for identifying which portion of the functionality is to be put in software. ... the attribute may further specify a target processor for processing the software implementing the portion of functionality").

Per Claim 16:

Aubury discloses:

- **wherein the set of parameters of the remote function call further comprises a reference to a memory location used for storing information on the return status of the function to be called** ([0186], "the processor starts with a definition of the instruction width, and the width of the internal memory and stack addresses. This is followed by an assignment of the processor opcodes").

Per Claim 17:

Aubury discloses:

- **wherein the target system further comprises a system memory and a system bus** (FIG. 21, [0339], "a number of other units interconnected via a system bus 2112");

- **the system memory, the first processor and the second processor being coupled by the system bus** (FIG. 21, [0039], "a central processing unit 2110, such as a microprocessor, and a number of other units interconnected via a system bus 2112... includes a Random Access Memory (RAM) 2114, Read Only Memory (ROM) 2116").

Per Claim 18:

Aubury discloses:

- **wherein the general-purpose processor is a digital signal processor** (FIG. 21, [0039], "a central processing unit 2110, such as a microprocessor, and a number of other units interconnected via a system bus 2112... includes a Random Access Memory (RAM) 2114, Read Only Memory (ROM) 2116").

Per Claim 19:

This is the compiler program product implementing all the steps of the method in claim 1, wherein all claimed limitation have been address and/or covered in cited areas as set forth in claim 1. Thus, accordingly, this claim is also anticipated by Aubury.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anna Deng whose telephone number is 571-272-5989. The examiner can normally be reached on Monday to Friday 9:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at 571 –272-3708. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anna Deng

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SPE 2191